In the Specification

Please amend the paragraph beginning at page 10, line 2 as shown:

The regions shown at 440 in Figure 4 can also be implanted to form lightly doped source/drain extension regions and/or halo implanted regions. The extensions as shown at 440 and halo implantation can be formed by dopant ion implantation before spacer 400 is formed. In addition, either or both n-type and p-type impurities can be implanted as needed to form the specific desired components. In a preferred embodiment where complementary metal oxide semiconductor (CMOS) technology is used, n-type dopants and p-type dopants must be implanted into respective portions of the substrate to form the source and drain regions of the NFETs and the PFETs. A sufficiently thick layer of polysilicon has the ability to block ion implantation into underlying layers. The sacrificial polysilicon gate ~~300~~ 210 and the spacers 400, 410 function together as an implant mask during ion implantations to form the source and drain regions.

Please amend the paragraphs beginning at page 10, line 15, continuing through page 12, line 9 of the Specification as shown:

As shown in Figure 6, the sacrificial gate 210 is then removed, as by RIE, stopping on the etch stop layer 200 so as to avoid damaging the surface of the substrate ~~200~~ 100 under which the conduction channel 630 of the transistor will be

formed. As a result, as shown in Figure 6, an opening 600 is formed, bound by the etch stop layer 200 and the sidewalls 610 of the L-shaped spacers 410.

Once the sacrificial gate 210 has been removed, a shallow threshold voltage adjustment implant can be performed through the etch stop layer 200. Thereafter, an anneal is performed to diffuse the dopant ions to the desired distribution and to repair damage to the crystal structure of the substrate ~~200~~ 100 as a result of the implant. Then, the etch stop layer 200 is removed, as by a dry directional etch selective to silicon and to nitride such as RIE.

Alternatively, a doped glass drive-in process is used to provide the threshold voltage adjustment to the transistor's conduction channel. In such process, the etch stop layer 200 is removed, as by a dry directional etch such as RIE. A thin layer of dopant material such as arsenic doped glass (if an n-type implant is desired) or borosilicate glass (if a p-type implant is desired) is then deposited onto the surface 700 of substrate 100 in the place of the etch stop layer 200 within the opening 600, as shown ~~at 700~~ in Figure 7. Thereafter, the dopant is distributed to the desired depth and distribution through a drive-in anneal. The doped glass material is then removed from the opening 600, as by a dry directional etch.

Whichever process is used to provide the threshold voltage adjustment, the surface 700 of the substrate ~~at 700~~ is now cleaned and the final gate dielectric 800 is now formed in the opening 600, as shown in Figure 8. In an embodiment, the gate

dielectric 800 includes an oxide layer and is thermally grown on the substrate 100 within the opening 600. In another embodiment, the gate dielectric 800 is formed by deposition, as by low pressure chemical vapor deposition (LPCVD) of a material such as silicon dioxide, silicon nitride, or silicon oxynitride. Other choices of materials exist for the gate dielectric. For example, a gate dielectric of hafnium oxide (HfO_2) or of zirconium oxide (ZrO_2) can be formed as a gate dielectric having a desirably high dielectric constant K, higher than that of either silicon dioxide, silicon nitride or silicon oxynitride. Such high-k gate dielectric may be advantageous for a particular application, such as where a thicker gate dielectric is needed to protect against dielectric breakdown but without sacrificing transistor switching performance.